Amendments to the Specification

Please replace the paragraph beginning on page 10, line 11, with the following:

Fig. 5 illustrates the exemplary table 60 of Fig. 4 placed within a sequence of instructions 62 and displayed as a graphics output 64 of a graphics rendering engine hereof. The graphics output 64 can be presented as a window or screen shot having various fields which can be selected by a user through a pointing device, such as a mouse or keyboard. Window 64 is shown to include five columns. Column 66 is a breakpoint area in which developers can select a particular line or field as a navigation breakpoint by clicking the mouse on the line of interest. In the example shown, the second line of column 66 is highlighted as being selected by a user. The highlighted field 67 can be highlighted with a particular color. Column 62 is described earlier as the addresses in memory for the lines of disassembled assembly code. Column 68 shows the pipeline stages for each of the lines of disassembled code. For example, the instruction addresses 0x1000-0x100[[4]]3 are within the execution stage of the processor pipeline, wherein the instruction at address 0x1002 can be a 32-bit instruction and thereby occupies addresses 0x1002 and 0x1003. The same can apply to address 0x1004. The pipeline information is shown presented for each line of assembly code. The ordering of instructions in the pipeline stages is presented in the context of the developer's code rather than in the context of the pipeline itself.